Design of the new MCM

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Abstract

The present MCM's will not meet DØ specifications when the Tevatron changes to operation with 132 ns bunch crossing. It has been decided to replace these modules. This note describes the design of the new MCM's. DØ note 3898.

1 Introduction

Visible Light Photons Counters (VLPC's) detect the light from the scintillators in the Central Fiber Tracker, and Central and Forward Preshower detectors of the DØ experiment. In total, these detectors have one hundred and one thousand channels. The VLPC output charge is currently amplified by a "SIFT" chip in a Multi Channel Module (MCM) on an Analog Front End board (AFE). The SIFT chips will not meet the DØ specifications when the Tevatron goes to operation with 132 ns bunch crossing.[1] The options are discussed in [2]. Finally it was decided to replace all MCM's on the AFE's. This note describes the design of the new MCM's.

2 The new MCM

The new MCM's are designed to be mechanically and electrically compatible with the old MCM's. They have 64 channels. Each channel integrates the charge of a VLPC and provides two outputs: a discriminator bit each bunch crossing time of 132 ns, and, upon L1 trigger accept, the amplitude (ADC with 10 bit resolution) and the discriminator bit again. The prototype MCM (less the custom AC chip) has been designed and simulated, and is currently being manufactured.

The new MCM has all of the functionality of the old MCM, and in addition, has functionality presently done by the AFE board: the "LVDS-MUX" and the "virtual SVX".

Mode	MODE0	MODE1
Initialize	0	0
Acquire	1	0
Digitize	1	1
Readout	0	1

Table 1: Four modes of operation of the new MCM.

The new MCM has a custom "AC" chip (currently being designed by Abderrezak Mekkaoui), two dual channel ADC's (Analog Devices AD9201), one Field Programable Gate Array (FPGA, Xilinx XC2S30 in a flat pack TQ144), and two low drop out voltage regulators (Texas Instruments REG104-3.3 and REG104-2.5 in DDPAK-5 packages). The design of the new MCM can be found in D0server4 → projects → TriggerElectronics → 132ns. The schematics of the new MCM can be found in → layout → Mcmii.dsn and opened with the Orcad Capture program. The Xilinx foundation schematics used to configure the FPGA can be found in → Xilinx → FPGA6_17AUG01.ZIP. The printed circuit board prototype layout can be found in → layout → MCMII_20010809.zip and viewed using the Orcad Layout and GC-Prevue programs.

The AC chip is CMOS with a 0.25μm, 2.5 V process. Chips on the AFE board use 3.3V. So all signals between the AC chip and the AFE board go through the FPGA for level translation. Signals between the AFE or the ADC's and the FPGA use the 3.3V LVTTL standard. Signals between the AC chip and the FPGA use the 2.5V LVCMOS2 standard.

The FPGA is configured in Slave-Parallel mode. Once the FPGA is configured, the new MCM operates in one of four modes controlled by the pins MODE0, MODE1 and CHANGE_MODE as shown in Table 1. The downward going transition of CHANGE_MODE latches the mode change.

The Initialize mode is used to configure the AC chip through the pins PRIORITY_IN (SPI_IN), SVX_CLK (SPI_CLK) and PRIORITY_OUT (SPI_OUT). In Aquire mode the new MCM outputs the discriminator bits over ten lines to the LVDS driver on the AFE board, the AC chip stores the analog data in a pipeline, and the FPGA stores the discriminator information in a pipeline awaiting a L1 trigger accept. Digitize Mode is set by a L1 trigger accept. During Digitize mode the analog data of the 64 channels of the selected event, stored in the analog pipelines of the AC chip, are read out of the AC chip over four balanced analog lines, digitized by the two dual channel ADC's, and formatted and stored in the Random Access Memory (RAM) of the FPGA together with the corresponding discriminator bits. In Readout Mode the ADC and discriminator information of the event selected by the L1 trigger

are read out. Details are given below.

3 Clocks

Four clocks are provided to the new MCM: CLK_8_PWM, CLK_30, CLK_53 used in Acquire and Digitize modes, and SVX_CLK used in the Initialize and Readout modes. The clocks used in the new MCM are shown in Figure 1. The clock CLK_8_PWM has a period of 132 ns, and a duty cycle that defines the charge integration window and the reset time of the AC chip. The clock CLK_30 has a period of 132/4 ns, and the clock CLK_53 has a period of 132/7 ns. For correct operation, the clocks CLK_8_PWM, CLK_30 and CLK_53 must maintain the phase relation shown in Figure 1 to within ± 5 ns. (See also the discussion in Appendix B.) The clock CLK_30 is used to generate all other clocks shown in Figure 1, with CLK_8_PWM used for synchronism. Several clock cycles are required to atain synchronism, so the clocks CLK_8_PWM, CLK_30 and CLK_53 should be applied with no interruption during the 4 modes of operation, even if not used during Initialize and Readout. The frequency of the SVX_CLK clock is less than approximately 32 MHz, but otherwise arbitrary.

4 The AC chip

The AC chip is currently under design, so all information on this chip is preliminary. The specifications of the chip are given in Appendix A. The 132 ns cycle has a charge integration window setable up to 86 ns (nominally 80 ns), and a reset time as short as 46 ns. The risetime of the preamplifier is approximately 10 ns, so the maximum window for full charge integration is $\approx 86 - 3 \times 10$ ns ≈ 56 ns. This point is further discussed in Appendix B. The duration of the integration window is determined by the duty cycle of the CLK_8_PWM clock. During the integration window there are no clock transitions to reduce interference. The AC chip has 32 discriminator output lines, with each line carrying the discriminator information of two channels time multiplexed during the reset interval using the DISC_1 and DISC_2 signals as discussed in Appendix B. The AC chip has a 64 channel analog pipeline with a depth programable from 0 to 48. The chip also has four 16-to-1 analog multiplexers. In the Digitize mode the analog data is read out over 4 balanced lines at 7.6 MHz to be digitized by the two dual channel ADC's. The output of the ADC's is transmitted to the FPGA over ten lines at 30 MHz.

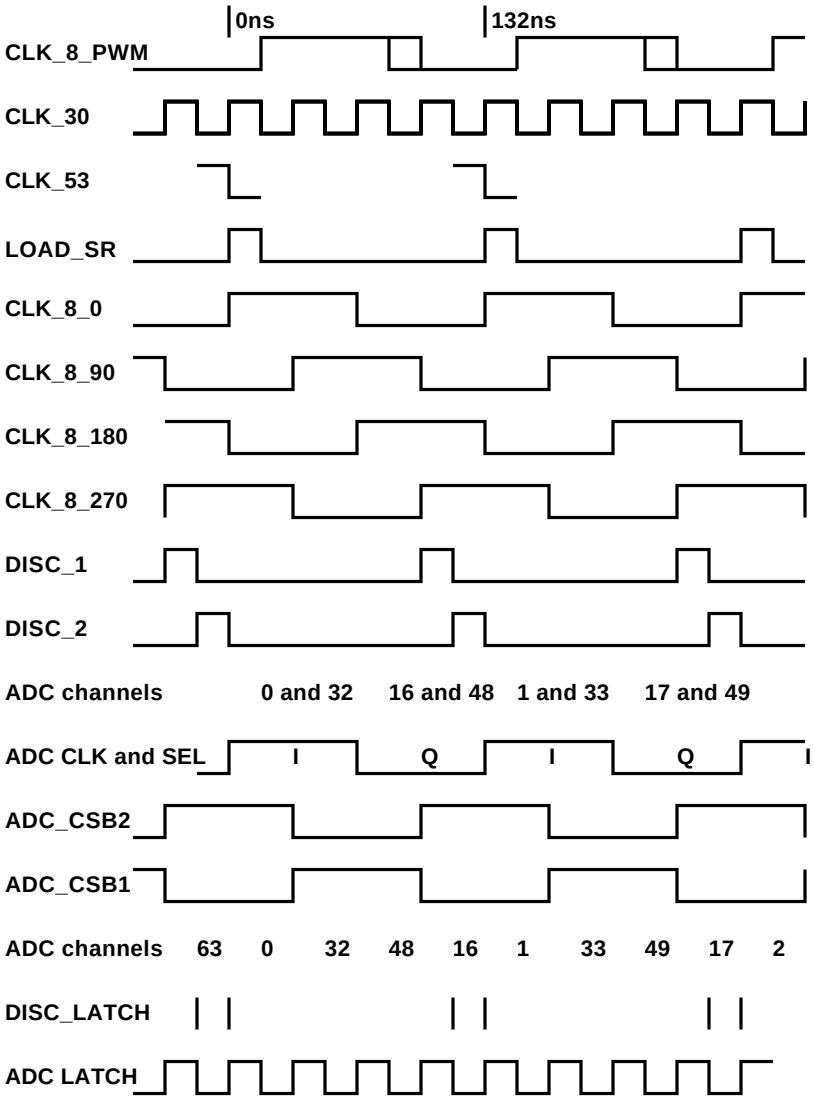

Figure 1: Clocks used in the new MCM. The clocks CLK_8_PWM, CLK_30 and CLK_53 must be provided to the new MCM with the phases indicated ± 5 ns.

5 FPGA configuration

The top level schematic of the FPGA configuration is fpga_top.sch. It contains six modules: MODE, CLOCKS, LVDS, DISC_PL, DIGITIZE and READOUT which can be found in corresponding schematics.

The module MODE latches the operating mode. The mode is determined by MODE0 and MODE1 as shown in Table 1. The mode is latched by the negative going edge of a CHANGE_MODE transition. The actual change of mode then occurs synchronously with the next positive going transition of the clock CLK_8_180. Care should be taken that the two transitions differ by at least the flop-flop setup time.

The module CLOCKS generates all clocks used by the FPGA as shown in Figure 1. The clock CLK_53 is used to read out the discriminator data to the LVDS driver on the AFE board. All other clocks shown in Figure 1 are generated from CLK_30 and synchronized by CLK_8_PWM. Two Digital Phase Locked Loops (DLL's) are used to obtain accurate 50% duty cycle square waves for the CLK_30 and CLK_53 clocks. It takes 4×132 ns to obtain synchronization.

The module LVDS latches two discriminator signals from each of 32 outputs of the AC chip every 132 ns. The 64 discriminator bits are then serialized into 10 streams and sent to the LVDS driver on the AFE board at 53 MHz. The order of the discriminator bits needs to be set for each MCM to comply with the trigger framework requirements.

The module DISC_PL loads the 64 discriminator bits into a digital pipeline. The module has two binary counters: I457 counts cyclically from 0 to 48 and determines the write address of the Random Access Memories (RAM). The counter I460 also counts cyclically from 0 to 48, but is delayed by the pipeline depth that can be set anywhere from 0 to 48. This counter determines the read address of the RAM. (The RAM capacity even permits setting the digital pipeline depth to 256, but this is not useful because the maximum analog pipeline depth of the AC chip is 48.) The change of mode from Acquire to Digitize freezes the delayed counter I460 which now points to the L1 accepted event.

The module DIGITIZE writes both the ADC and discriminator data of the L1 selected event to RAM in the order to be read out during the Readout mode. The channels to be Read out can be chosen as follows: (1) All channels; (2) Hit channels; (3) Hit channels and nearest neighbors; or (4) Hit channels and nearest neighbors and first and last. A hit channel is a channel that has either a discriminator bit set, or the ADC is above a programable threshold. The DIGITIZE module has four 16-to-1 digital multiplexers for discriminator bits that mirror the four 16-to-1 analog multiplexers of the AC

chip. This module also has a 4-to-1 digital multiplexer that mirrors the multiplexing of the two dual channel ADC's. Thus (we hope) the ADC channels and the discriminator bits will be readout in the same order as designed. However, since the AC chip design has not been finalized it might be necessary to reorder the discriminator channels in the DIGITIZE module. Any order can be chosen.

The operation of the FPGA in Digitize and Readout modes is summarized in Figure 2. The DIGITIZE module has three binary counters clocked by CLK_30. H21 is used to delay the enable of counters H18 and H19. This is done to offset the delay in the AC chip (unknown at this time) and the delay in the ADC chips (three 132 ns clock cycles). H18 is the RAM address counter, and H19 is the channel number counter. Counter H18 is enabled one clock cycle before H19. This is done so that the first channel selected for readout is written to address 1, not 0. Channel zero of RAM I638 is reserved for CHIP_ID. Channel zero of RAM I640 is reserved for STATUS (currently set to zero). This information is put into RAM during the FPGA configuration by setting the parameter INIT of the RAM's.

The ADC's have 10 bit resolution. This resolution is needed in order to callibrate the detectors observing the single-photoelectron peaks using light from Light Emitting Diode's (LED's). In order to pack 10 bits into one byte we have proceeded as follows. On "large signals" we transmit the 7 **most** significant bits, followed by a 0. For "small signals", *i.e.* those signals that have the three most significant bits equal to zero, we transmit the 7 **least** significant bits, followed by a 1.

The READOUT module is responsible for the Readout mode. It is driven by the SVX_CLK clock. First, all MCM's are set into Readout mode. Readout control is a Daisy-Chain. When one MCM receives a PRIORITY_IN low signal its tri-state output takes control of the 8-bit bus and the contents of RAM's I638 and I640 are read out on alternate half-cycles of the SVX_CLK clock: I638 when the clock is high, and I640 when the clock is low. The output order of the bytes can be read off Table 2. Once the last channel is read out, control of the output bus is released and PRIORITY_OUT is set low to pass control of the bus to the next MCM. Simulations with the FPGA configured with no speed optimization indicate that Readout will be possible up to 64 MHz (with the SVX_CLK at 32 MHz). The actual maximum will depend on the output bus capacitance. Therefore reading out all channels requires $\approx 2\mu$s for each of 8 MCM's. Therefore $\approx 18\mu$s are required for Digitize and Readout if all channels are read out. With zero supression the readout time is of course less.

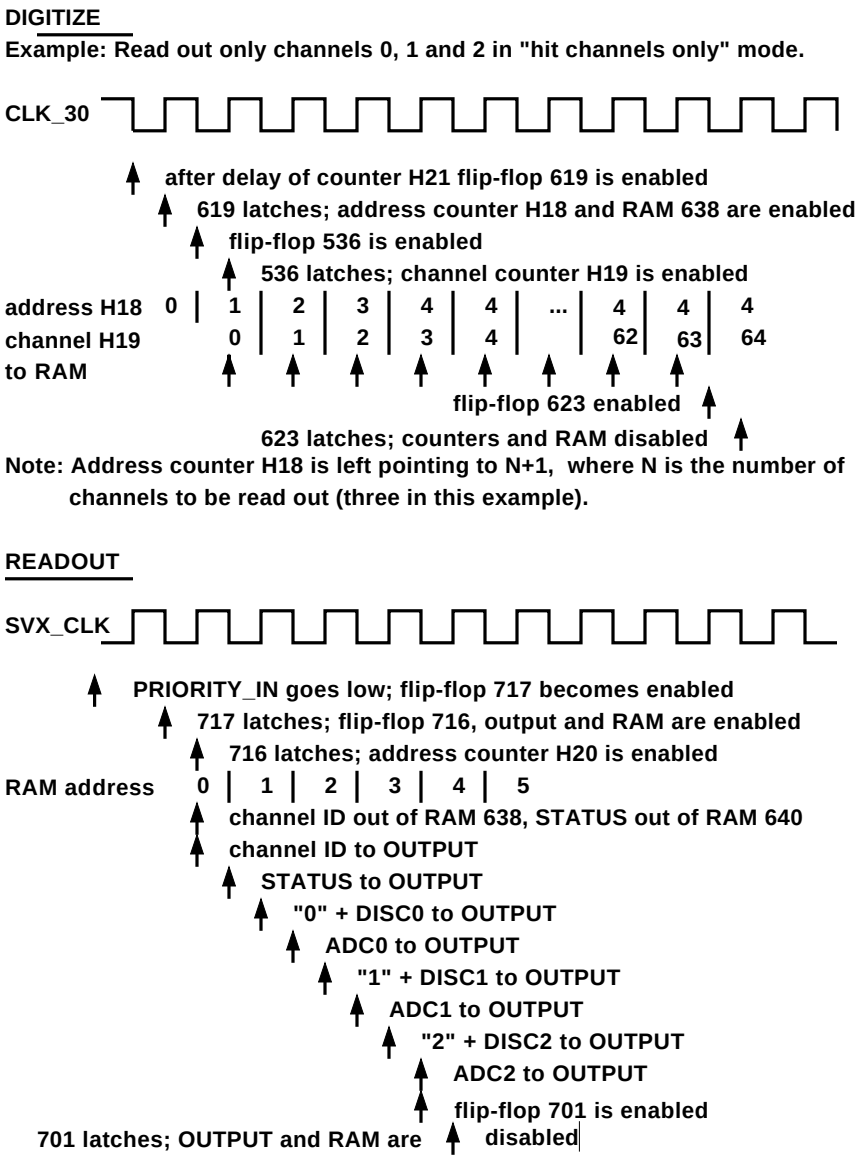

Figure 2: Timing during DIGITIZE and READOUT modes.

Address	RAM I638	RAM I640
0	CHIP_ID	STATUS
1	CH+D of channel 0	P_ADC of channel 0
2	CH+D of channel 1	P_ADC of channel 1
...		
64	CH+D of channel 63	P_ADC of channel 63

Table 2: Contents of RAM's I638 and I640 after the Digitize mode ends. "CH+D" means "channel number (7 bits) plus discriminator bit". "P_ADC" means "pseudo floating point ADC (7+1 bits)" as explained in the text. This Table asumes that all channels are being read out.

6 Power Supplies

The new MCM uses the power supplies shown in Table 3. The currents listed in the Table are estimates (they depend on the final design of the AC chip and on the capacitances of the loads) and should be measured.

7 Comissioning

Some parameters depend on the design of the AC chip which is not yet available, or depend on the system. The following parameters must be set at a later date:

- The delay provided by the counter H21 in the DIGITIZE module to obtain synchronism of counter H19 with the ADC data.
- The channels to be read out: (1) All; (2) Hit channels; (3) Hit channels and nearest neighbors; or (4) Hit channels and nearest neighbors and first and last. These options are set by the control lines of the multiplexer I470.
- The configuration of each MCM must put into RAM I638 the corresponding CHIP_ID number.
- The trigger framework requires a different order of the discriminator bits sent over ten lines to the LVDS driver on the AFE board. The order of the bits is chosen in the module LVDS.
- There is a large book-keeping task to produce configuration files for each MCM with the correct CHIP_ID, order of LVDS bits, and mode of channel readout.

Power supply	old MCM	new MCM	Load	Current
VDD_A	5.0V	2.5V	AC preamplifier	100mA
AVDD	5.2V	2.5V	AC pipeline amplifier	100mA
AVDD2	3.5V	3.5V	ADC analog	80mA
VDD_D	5.0V	5.0 or 3.3V	ADC digital	80mA
			FPGA HV	100mA
			FPGA LV*	250mA
			AC digital*	100mA

Table 3: Power supplies used by the new MCM. The currents are estimated upper bounds. The voltages presently provided by the AFE must be changed as shown. Loads with a * have a 2.5V low dropout regulator on the MCM.

- The phase of CLK_30 relative to the CLK_8_PWM clock determines the time between DISC_2 output and the beginning of charge integration as explained in Appendix B. This time should be set as required by the AC chip.

- The 3.3V LVTTL outputs of the FPGA can be set to "slow" or "fast", and their currents can be set from 2mA to 24mA. Currently we chose "slow" and 12mA. Also a programable delay can be inserted in the inputs to the FPGA. The optimum settings are system dependent and should be chosen during commisioning: choose the slowest transition that still gives a "nice" waveform.

- The new MCM was designed with flexibility in mind. Zero ohm and infinity ohm resistors permit choosing parallel or serial configuration of the FPGA, permit setting the input voltage span of the ADC's, and permit choice of 5V or 3.3V VDD_D operation. Also the reference voltage for the AC chip can be set with resistors.

- During commisioning two internal signals of the FPGA can be connected to two spare output pins. In normal operation the DLL_LOCKED signal should be connected to one of these pins.

- In the final configuration of the MCM and AFE care should be taken to leave no dangling inputs or undefined outputs as oscillations and overheating might occur. Also place 0V (low) outputs on AFE board CPLD's connected to lines that are grounded on the new MCM's.

8 Layout

The layout has six layers of which only two have signal traces. Layer 1 (the top layer) has the 64 input analog lines, the 32 discriminator lines, the 10-line ADC bus, and all components. The "last" analog line and the "first" discriminator line are separated by an AC analog ground island to reduce their capacitive coupling. Furthermore the discriminator lines only switch during the reset period of the preamplifiers.

Layer 2 has three ground planes: (1) AC analog ground, (2) ADC analog ground, and (3) Digital ground. The AC and ADC analog grounds are not connected to avoid ground loops. The four analog inputs to the ADC chips are balanced. The corresponding outputs of the AC chip have one lead decoupled to AC analog ground. This line carries a reference voltage from the ADC chip. To reduce offset, the AC chip output will (we hope) have double correlated sample. The common mode between AC and ADC analog grounds is rejected by the balanced ADC inputs.

The advantage of having all lines on both sides of the same ground plane is that return currents on the ground planes can flow near the lines (passing from one side to the other side of the ground plane through the holes left by the vias), thus reducing inductance.

Layer 3 has the 10 LVDS outputs, the 8 L1 accepted data output bus, the lines to configure the FPGA, the four balanced analog lines from AC to ADC, and clock lines.

Layers 4, 5 and 6 contain ground planes, power supply planes and power supply leads. An AC analog ground plane was put on layer 4 under the corresponding plane in layer 2. This way "quiet" lines can be placed in case the designer of the AC chip finds difficulties acomodating the order of pads we have assumed.

Finally we placed low impedance decoupling capacitors near **each** power supply pin of each chip.

The prototype layout uses 6 mil traces with 6 mil spacing. Once the final footprint of the AC chip becomes known, 3 mil traces will have to be used near the AC chip. The metalization has "0.5 oz copper" and layer 1 is gold plated. For best performance the AC chip should be directly bonded to the MCM with no packaging (and, furthermore, a 144 pin flat pack will not fit mechanically on the MCM).

9 Conclusions

The AC chip is currently being designed. The prototype MCM has been designed and simulated, and is being manufactured. The new MCM has a flexible, conservative and robust design that will meet all DØ requirements.

A Specifications of the AC chip

- Bunch crossing rate = 132 ns.
- Channels = 64 trigger + 64 analog.
- Window for charge collection: from 50 to 86 ns controlable by width of clock pulse. The effective window is less due to preamplifier risetime of approximately 10 ns as discussed in Appendix B.
- Temperature range = 10^oC to 50^oC.
- Five gain settings (G, G/2, G/4, G/8, G/16).
- Input signal from Fiber Tracker or MIP layer of Preshower Detector (at high gain):

  Minimum: 1 photoelectron at 90 degrees incidence = 4 to 9 fC

  Typical: 1 MIP = 7 photoelectrons = 45 fC for Fiber Tracker; 1 MIP = 65 fC for MIP layer of Preshower Detector

  Maximum before saturation = 300 fC

  Note: These, and all charges throughout this document, are at the VLPC. The interconnect from the VLPC's and the AC chip is described below.

- Threshold setting for Fiber Tracker and MIP layer of Preshower Detector (at high gain):

  from 0 to 100 fC with 7 bit control (linear)

  Typical: 4 to 20 fC

  99% of channels within $\pm$4 fC.

  Rms noise $<$ 0.8 fC.

  Temperature coefficient $<$ 2 fC/10^oC.

- Input signal from shower layer of Preshower Detector (at low gain = high gain/16):

  Typical: One 40 GeV electron or gamma at 45 degrees = 25 MIP per strip = 450 photoelectrons = 1890 fC.

  Maximum before saturation = 5000 fC

- Threshold setting for shower layer of Preshower Detector (at low gain = high gain/16):

  From 0 to 1600 fC with 7 bit control (linear)

  Typical: 100 to 750 fC.

- Power consumption < 10 mW per channel.

- Inputs:

  VLPC's in a cryostat, connected to the AFE with a high density interconnect (described below), byased to approximately +7V through a 100 K resistor, and a 100 pF series capacitor, both on the AFE board. The VLPC is an ideal current source. The voltage of the input pulse is NEGATIVE going. The input stray capacitance to ground is 30 to 40 pF as described in more detail below.

  64 signal channels.

  The connections from the AFE board to each MCM mounted on the AFE has 13 ground leads (one each 6 channels except on the edges), see the MCM footprint. The AC chip footprint should have corresponding ground pads.

  The kapton high density interconnect has a single copper layer. It has 64 signal traces alternated with 65 ground traces. Each trace is 3 mil wide. The spacing is 9.5 mil from center of signal trace to center of ground trace. The thickness of the copper traces is 0.005 millimeters. The length of the interconnect is 16.25 inches. The capacitance of signal trace to ground is 23 ± 3 pF. Additional stray capacitance on the AFE and MCM is approximately 10pF. The characteristic impedance of the transmission line is $Z_0 = 122 \pm 5$ ohm. The resistance of a signal trace is 13 to 28 ohm.

  Cross-talk due to uneven injection of MOS_FET switching charge into input lines should not exceed 2 fC.

- Analog outputs:

  64 channels with 4 16:1 analog multiplexers.

Outputs are "pseudo" balanced. One lead has an external reference voltage decoupled to AC anlog ground to be used for double correlated sample to reduce output offset. The ADC inputs are balanced.

Readout occurs in readout mode (not during acquisition mode).

Readout rate = 7.6 MHz.

Channel uniformity should be within ±3%, *i.e.* $\pm 0.03 \times 300$ fC = ±9 fC referred to the input at high gain.

Rms noise < 0.8 fC referred to the input.

Temperature coefficient < 2% of full scale per 10^oC.

External load approx 10 pF.

Internal compensation of MOS switching charges (if possible).

- Digital outputs:

  64 channels with 2:1 digital multiplexing for 32 unbalanced outputs.

  Output in acquisition mode and only during integrator reset.

  Standard: LVCMOS2, 2.5V.

  External load ≈ 10 pF.

- Test input:

  Negative charge from 0 to 500 fC (for gain G) or 0 to 8000 fC (for gain G/16) controlled by CAL.

  Pulse time and width determined by CAL-INJECT.

  Pattern settable with shift register 64 bits deep.

- Pipeline depth:

  48 buckets programable from 0 to 48.

- Power supply: +2.5V, digital separate from analog(s).

  Power supplies should require no sequencing.

- Clocks provided to AC chip (polarities are flexible):

  1) 132 ns period with settable duty cycle, LVCMOS2 high (approx. 2.5V) for charge acquisition window, LVCMOS2 low (approx. 0V) for reset.

  2) LVCMOS2 high during discriminator bucket 1 readout.

  3) LVCMOS2 high during discriminator bucket 2 readout.

All other clocks needed in the chip for acquisition and readout to be derived from these.

- Analog output will be digitized by ADC AD9201 of Analog Devices. The input voltage span of the ADC is 0.3 to 1.3V. The output of the AC chip will be referenced to VR which is provided to the AC chip from VREF = 1V of the FADC and a resistor divider. We will set VR = 0.4V if the output is positive going (preferred), or VR = 1.2V if the output is negative going. Therefore the dynamic range will be 0.9V. VR will be decoupled to the AC chip analog ground, not to the ADC analog ground, to reduce common mode noise.

- Decoupling capacitors: The inputs to the AC chip are negative going. Therefore the VLPC charge loop includes AVDD and AGND. Therefore several AGND-AVDD pad pairs will be needed to place decoupling capacitors.

- The AC chip has four operating modes controlled by the signals (MODE0, MODE1) as follows: (0, 0) for INITIALIZE, (1, 0) for ACQUIRE, (1, 1) for DIGITIZE, and (0, 1) for READOUT. The change of modes occurs on the edge of negative going transitions of the CHANGE_MODE signal.

B A discussion on preferred clocks:

Two alternatives are considered. The preferred alternative (1) is to use the 30MHz clock. Then the timing of discriminator outputs is as shown in Figure 3.

In this alternative the window is 132 - 46 = 86ns. Let us asume that the integration time constant is 10ns. Then the fraction of charge integrated as a function of arrival time is

56 ns 95%
66 ns 86%

Should the need arise we might try the same but using the 53MHz clock. In this case (2) the discriminator valid widths are 9.4ns instead of 16.5ns, and the reset pulse can be as short as 32ns. In this alternative the window is 132 - 32 = 100ns. Then the fraction of charge integrated as a function of arrival time is

60 ns 98%
70 ns 95%

Alternative 2 fully meets the specs. However I believe alternative 1 still meets our needs. My choice, at least for initial commisioning, is alternative 1.

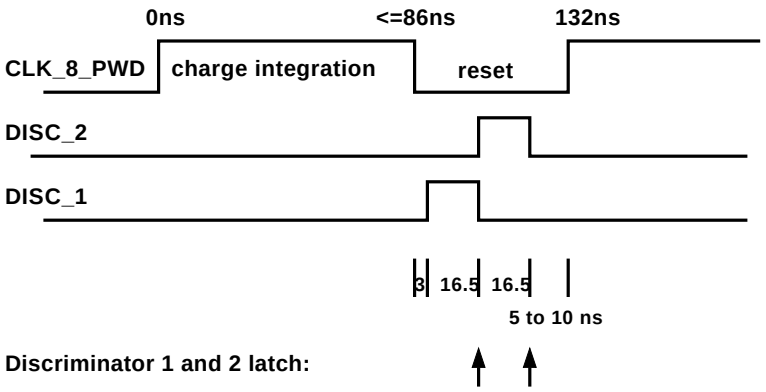

Figure 3: Maximum charge integration window, AC chip discriminator outputs, and FPGA discriminator latches. The phase of the clock CLK_8 relative to CLK_8_PWM determines the time from the end of the DISC_2 signal to the beginning of charge integration.

This alternative 1 is more robust and simpler to operate because it depends on only one clock and this clock is of lower frequency. The chip should be designed for alternative 1 with a safety margin. Keep in mind that we might, at a later time, atempt 53MHz operation and shorten the reset time somewhat in the unlikely case that the need arises.

References

[1] P. Rubinov and B. Hoeneisen, DØ note 3897.

[2] B. Hoeneisen and Paul Rubinov, DØ note 3773.